REMARKS

Claims 1-13 were rejected. Claims 1-3, 10 and 11 have been amended. Therefore, upon entry of this response, claims 1-13 will be pending in the application.

Claims 1-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,140,704 ("Ueno") in view of U.S. Patent No. 6,061,279 ("Toda"). Applicant respectfully submits that claims 1-13 are patentable over Ueno in view of Toda because neither reference, either alone or in combination, discloses every limitation recited in independent claims 1-3.

For example, claim 1, as amended, recites an amplifier for amplifying a noise component output from a highpass filter. Claim 2 and 3, as amended, recite an amplifier circuit for amplifying the noise component output from the noise extracting circuit. Claims 1-3, as amended, also recite a time constant circuit for smoothing the amplified noise component with a predetermined time constant and for generating a control voltage that is applied to the amplifier. The time constant circuit includes a first capacitor, a charge circuit for charging the first capacitor, a discharge circuit for discharging the first capacitor and a charge/discharge speed setting unit that causes a difference between a charge speed of the charge circuit and a discharge speed of the discharge circuit.

In contrast, Ueno discloses a pulse noise suppression system that includes highpass filter 3, noise amplifier 4 and rectifier circuit 5. (*Ueno* – col. 3, lines 63-68). A noise component that passes through highpass filer 3 is amplified by noise amplifier 4 and rectified by rectifier circuit 5, which then outputs an automatic gain control (AGC) signal to noise amplifier 4. (*Ueno* – col. 1, lines 21-26 and lines 45-49). According to Ueno, when the noise level increases, the AGC signal lowers the gain on noise amplifier 4. (*Ueno* – col. 1, line 68; col. 2, line 1). Ueno does not disclose how the AGC signal is controlled. Toda discloses a delay circuit that stores analog signals in memory cells M1-Mn in a predetermined input sequence via input switches SW1-SWn, capacitors C1-Cn, and control signals ϕ1-ϕn. (*Toda* – col. 6, lines 34-47). The delay circuit also outputs the signals in a predetermined output sequence via output switches SW1'-SWn' and control signals ϕ1'-ϕn'. (*Toda* – col. 6, lines 34-47). Thus, applicant respectfully submits that neither Ueno nor Toda disclose a time constant circuit for smoothing an amplified noise component with a predetermined time

constant, much less a time constant circuit that includes a first capacitor, a charge circuit, a discharge circuit and a charge/discharge speed setting unit.

Accordingly, applicant respectfully submits that independent claims 1-3 are patentable over the cited references and are allowable. As claims 4-13 depend from claim 1, applicant further submits that dependent claims 4-13 are likewise allowable. Reconsideration of the application and an early Notice of Allowance are respectfully requested.

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